LISTING OF THE CLAIMS (1-21)

Claim 1 (currently amended): A circuit for controlling a rise-time of a signal, comprising:

a voltage multiplication circuit which converts an input voltage to an output voltage greater than said input voltage;

a ~~switched capacitor circuit~~ ramp generator coupled to said voltage multiplication circuit which controls said output voltage from said voltage multiplication circuit, wherein a ratio between a first capacitor of said ramp generator ~~switched capacitor circuit~~ and a second capacitor of said ramp generator ~~switched capacitor circuit~~ determines said rise-time of said signal~~, said circuit for controlling a rise time of a signal further comprises a constant ramp generator~~.

Claim 2 (original): The circuit of Claim 1, wherein said voltage multiplication circuit comprises a charge pump.

Claim 3 (original): The circuit of Claim 1, wherein said signal is used to program and erase Flash EPROM cells.

Claim 4 (canceled)

Claim 5 (original): The circuit of Claim 1, wherein said signal comprises a staircase ramp signal.

Claim 6 (canceled)

Claim 7 (currently amended): The circuit of Claim 1 further comprising a level shifter ~~to shut off said signal~~.

Claim 8 (original): The circuit of Claim 1 further comprising two non-overlapping clock signals.

Claim 9 (currently amended): The circuit of Claim 1 further comprising a ring oscillator coupled to said ramp generator ~~switched capacitor circuit~~.

Claim 10 (currently amended): The circuit of Claim 1 further comprising a capacitor divider network coupled to ~~said~~a switched capacitor ~~circuit~~network.

Claim 11 (currently amended): The circuit of Claim 10, wherein said switched capacitor ~~circuit~~ network switches between ground and a node of said capacitor divider network~~divider node which has a constant reference voltage according to a feed back system~~.

Claim 12 (currently amended): The circuit of Claim 11, wherein said node is coupled to~~feedback system comprises~~ a CMOS comparator.

Claim 13 (original): The circuit of Claim 1 further comprising a divide by N counter.

Claim 14 (previously amended): A switched capacitor controller for controlling a rise time of an on-chip generated voltage source, comprising:

a charge pump;

a ramp generator coupled to said charge pump, wherein said ramp generator comprises a switched capacitor;

a regulator circuit coupled to said switched capacitor circuit which causes a capacitor to switch between ground and a node, wherein a stair-step ramp signal is generated and said rise time is controlled according to said switched capacitor.

Claim 15 (original): The switched capacitor controller of Claim 14, wherein said rise time is controlled according to a ratio of two capacitors.

Claim 16 (original): The switched capacitor controller of Claim 14, wherein said on-chip generated voltage source is used to program a Flash memory.

Claim 17 (original): The switched capacitor controller of Claim 14 further comprising an oscillator coupled to said charge pump which generates an oscillating signal input to said charge pump.

Claim 18 (original): The switched capacitor controller of Claim 17 further comprising:

a divider coupled to said oscillator;

a non-overlapping two phase clock generator coupled to said divider.

Claim 19 (original): The switched capacitor controller of Claim 14, wherein said ramp generator further comprises a capacitor divider network.

Claim 20 (currently amended): In a flash memory, a method for controlling a rise time of an on-chip generated voltage source used to program said flash memory, comprising:

generating a programming voltage VPP from a power supply, wherein said programming voltage is greater than voltage VCC from said power supply;

activating a program signal to program a cell of said flash memory;

generating a stair-case ramp based on said programming voltage in response to said program signal, wherein steps of said stair-case ramp have a period corresponding to a clock signal and voltage increases corresponding to a reference voltage times a ratio of two capacitor values.

Claim 21 (original): The method of Claim 20 further comprising the step of switching a capacitor between ground and a node voltage to generate said staircase ramp.